THAT WHICH IS CLAIMED IS:

1. A method of routing network-based data arranged in frames comprising the steps of:

receiving a first portion of a frame within a FIFO receive memory of a network device, wherein the first portion of the received frame includes data having preselected address fields;

transferring a burst of data, including preselected address fields, from the FIFO receive memory to an external shared system memory that exists between the network device and a host processor;

generating an interrupt signal to the host processor indicative that the preselected address fields of the frame are present in the shared system memory; and

initiating within the host processor an address and look-up algorithm in address tables to determine frame routing based on the preselected address fields.

2. A method of routing according to Claim 1, and further comprising the step of transferring data from the FIFO receive memory through a direct memory access unit of the network device.

3. A method of routing according to Claim 2, and further comprising the step of generating an interrupt signal to the host processor from the direct memory access unit after the direct memory access unit has transferred data to the shared system memory.

4. A method of routing according to Claim 1, and further comprising the step of selecting the amount of data to be transferred from the FIFO

receive memory based on the desired address fields to be analyzed by the host processor.

5. A method of routing according to Claim 1, and further comprising the step of receiving the balance of the frame completely within the shared system memory.

6. A method of routing according to Claim 5, and further comprising the step of generating an end-of-frame interrupt when a frame has been completely received within the shared system memory.

7. A method of routing according to Claim 1, and further comprising the step of generating a start-of-packet interrupt to a communications processor within the network device when the data received within the FIFO receive memory has reached a desired watermark value.

8. A method of routing according to Claim 7, and further comprising the step of issuing a command to a direct memory access unit of the network device to transfer data from the FIFO receive memory to the shared system memory after the communications processor has received the start-of-packet interrupt.

9. A method of routing according to Claim 8, and further comprising the step of arbitrating use of a system bus between the direct memory access unit and a bus arbitration unit.

10. A method of controlling network data flow arranged in frames comprising the steps of:

receiving at least a first portion of a frame containing data receive memory of a network device,

wherein the first portion of the received frame includes data having preselected address fields;

transferring a burst of data, including preselected address fields, from the FIFO receive memory to a shared system memory that exists between a host processor and the network device; and

generating an interrupt signal to the host processor indicative that the preselected address fields of the frame are present in the memory.

11. A method according to Claim 10, and further comprising the step of transferring data from the receive memory through a direct memory access unit.

12. A method according to Claim 11, and further comprising the step of generating an interrupt signal to the host processor from the receive memory after the direct access memory unit has transferred data to the shared system memory.

13. A method according to Claim 10, and further comprising the step of selecting the amount of data to be transferred from the receive memory based on the desired address fields to be analyzed by the host processor.

14. A method according to Claim 10, and further comprising the step of receiving the balance of the frame completely within shared system memory.

15. A method according to Claim 10, and further comprising the step of generating an end-of-frame interrupt when a frame has been completely received within shared system memory.

16. A method according to Claim 10, and further comprising the step of generating a start-of-

packet interrupt to a communications processor when the data received within the receive memory has reached a desired watermark value.

17. A method according to Claim 10, and further comprising the step of issuing a command to a direct memory access unit of the network device to transfer data from the receive memory to the shared system memory after the communications processor has received the start-of-packet interrupt.

18. A method according to Claim 10, and further comprising the step of arbitrating use of a system bus between the direct memory access unit and a bus arbitration unit.

19. A method of routing network-based data arranged in frames comprising the steps of:

receiving at least a first portion of a frame within a FIFO receive memory of a network device, wherein the first portion of the received frame includes data having preselected address fields;

selecting the amount of data to be transferred from the FIFO receive memory based on the desired address fields to be analyzed by a host processor;

transferring a burst of data, including preselected address fields, from the FIFO receive memory to a shared system memory that exists between the network device and the host processor;

generating an interrupt signal from the network device to the host processor indicative that the preselected address fields of the frame are present in the shared system memory; and

initiating an address and look-up algorithm to determine frame routing based on the preselected address fields.

20. A method of routing according to Claim 19, and further comprising the step of transferring data from the FIFO receive memory through a direct memory access unit of the network device.

21. A method of routing according to Claim 20, and further comprising the step of generating an interrupt signal to the host processor after the direct access memory unit has transferred data to the shared system memory.

22. A method of routing according to Claim 19, and further comprising the step of receiving the balance of the frame completely within the shared system memory.

23. A method of routing according to Claim 22, and further comprising the step of generating an end-of-frame interrupt when a frame has been completely received within shared system memory.

24. A method of routing according to Claim 19, and further comprising the step of generating a start-of-packet interrupt to a communications processor of the network device when the data received within the FIFO receive memory has reached a watermark value.

25. A method of routing according to Claim 24, and further comprising the step of issuing a command to a direct memory access unit of the network device to transfer data from the FIFO receive memory to the shared system memory after receiving the start-of-packet interrupt.

26. A method of routing according to Claim 19, and further comprising the step of arbitrating use of a system bus between the direct memory access unit and a bus arbitration unit of the network device.

27. A system for routing network-based data arranged in frames comprising:

a FIFO receive memory of a network device for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;

a host processor;

a shared system memory that exists between the network device and host processor for receiving data, including the preselected address fields, from the FIFO receive memory;

a direct memory access unit for transferring a burst of data from the FIFO receive memory to the shared system memory; and

a communications processor for selecting the amount of data to be transferred from the FIFO receive memory to the shared system memory based on the desired address fields to be analyzed by the host processor.

28. A system according to Claim 27, and further comprising an interrupt bus connected between the FIFO receive memory and communications processor, wherein said FIFO receiver memory includes an interrupt generator for generating an interrupt to the communications processor along the bus.

29. A system according to Claim 27, and further comprising a FIFO bus between the direct memory access unit and the FIFO receive memory on which data is transferred from the FIFO receive memory and through

the direct memory access unit to the shared system memory.

30. A system according to Claim 27, and further comprising a controller bus connected between the communications processor and the direct memory access unit through which data transfer commands are issued from the communications processor to the direct memory access unit to transfer data.

31. A system according to Claim 27, wherein said FIFO receive memory has a watermark value, and means for issuing a start-of-packet interrupt to the communications processor when the watermark value is reached.

32. A system for routing network-based data arranged in frames comprising:

a host processor for analyzing transferred bursts of data and initiating an address and lookup algorithm for dispatching a frame to a desired destination;

a shared memory for receiving data, including any preselected address fields; and

a network device having:

a plurality of ports, each port including a FIFO receive memory for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;

a direct memory access unit for transferring a burst of data from the receive memory to the shared system memory; and

a communications processor for selecting the amount of data to be transferred from the receive memory based on the desired address fields to be analyzed by the host processor.

33. A system according to Claim 32, and further comprising an interrupt bus connected between the FIFO receive memory and communications processor, wherein said HDLC ports include an interrupt generator for generating an interrupt to the communications processor along the bus.

34. A system according to Claim 32, and further comprising a FIFO bus connected between the direct memory access unit and the receive memory on which data is transferred from the receive memory and through the direct memory access unit to the shared system memory.

35. A system according to Claim 32, and further comprising a controller bus connected between the communications processor and the direct memory access unit through which data transfer commands are issued from the communications processor to the direct memory access unit to transfer data.

36. A system according to Claim 32, wherein said receive memory has a watermark setting at which the HDLC port issues a start-of-packet interrupt to the communications processor.

37. A system according to Claim 32, wherein said receive memory comprises a first-in/first-out (FIFO) receive memory.

38. A network controller having:

a plurality of ports, each port including a FIFO receive memory for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;

a direct memory access unit for transferring a burst of data from the FIFO receive memory to an external system memory jointly shared with a host; and

a communications processor for selecting the amount of data to be transferred from the FIFO receive memory based on the desired address fields to be analyzed by a host processor.

39. A network controller according to Claim 38, and further comprising an interrupt bus connected between the FIFO receive memory and communications processor, wherein said ports include an interrupt generator for generating an interrupt to the communications processor along the bus.

40. A network controller according to Claim 38, and further comprising a FIFO bus connected between the direct memory access unit and the FIFO receive memory on which data is transferred from the FIFO receive memory and through the direct memory access unit to a shared system memory.

41. A network controller according to Claim 38, and further comprising a controller bus connected between the communications processor and the direct memory access unit through which data transfer commands are issued from the communications processor to the direct memory access unit to transfer data.

42. A network controller according to Claim 38, wherein said receive memory has a watermark setting at which the port issues a start-of-packet interrupt to the communications processor.

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